UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/827,360	04/20/2004	Richard Carl Phelps	0120-030	2608

42015 7590 05/31/2005

POTOMAC PATENT GROUP, PLLC
P. O. BOX 270
FREDERICKSBURG, VA 22404

EXAMINER	
CLEARY, THOMAS J	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 05/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/827,360	PHELPS ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☒ Claim(s) *4,7,8 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/787,353.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20041215*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of Applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 09/787,353, filed on 16 March 2001.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the Applicant regards as his invention.

3. Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

4. In reference to Claim 1, it is unclear if the "bus connection units" of Line 10 refer to the same units as the "bus connecting unit" of Lines 13-14.

5. In reference to Claim 2, it is unclear as to what attributes the output circuitry is optimized for. There are various attributes, including, but not limited to, switching

speed, power consumption, and drive capability, to which the output circuitry can be optimized for.

6. In reference to Claim 8, it is unclear where the "one pipeline stage" is defined, based on the limitation "one pipeline stage, as herein defined" in Line 19. There is no prior definition of the term "pipeline stage" in the claims. Claim 8 is further indefinite in that it fails to point out what is included or excluded by the claim language "one pipeline stage, as herein defined". This claim is an omnibus type claim.

7. In reference to Claim 10, it is unclear if the apparatus comprises read, write, and transaction buses that are separate from the pipeline bus architecture, or if the pipeline bus architecture comprises separate read, write, and transaction buses.

Claim Objections

8. Claims 4, 7, 8, and 10 objected to because of the following informalities: Claim 4 appears to have used the word "or" in place of the word "of" in Line 31 and Claim 10 appears to have erroneously included the word "any" in Line 25. Appropriate correction, if necessary, is required.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1, 2, 3, 5, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over "Automatic High Level Synthesis of Partitioned Busses" by Christian Ewering ("Ewering") and US Patent Number 5,920,894 to Plog et al. ("Plog").

11. In reference to Claim 1, Ewering teaches an apparatus for use in a computer system comprising: a pipeline bus architecture, in which data traverses the bus architecture over a plurality of system clock cycles (See Figures 1 and 2 and Page 306 Column 2 Section 'Differential Equation'); a plurality of modules connected to the bus architecture (See Figure 1); wherein the bus architecture comprises: a plurality of bus connection units (See Figure 1 'Switch'); and a plurality of bus portions arranged in series, each bus portion, except the last in the series, being connected to the next portion in the series by way of a bus connecting unit (See Figure 1 'Bus Segment'), wherein each of the modules is connected to the bus architecture by way of a respective one of the bus connection units (See Figure 1). Ewering does not teach that each of the bus connection units includes multiplexer circuitry for selectively connecting a module to the bus architecture. Plog teaches connecting a plurality of devices to a bus using a multiplexer (See Column 5 Lines 50-54).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Ewering using the multiplexers of Plog, resulting in the invention of Claim 1, because multiplexers are a type of switch and to allow multiple units to be on the same segment of bus by allowing them to be connected in parallel fashion by connecting one unit to the bus at a time (See Column 5 Lines 50-54 of Plog), and thus increase the functionality by allowing a single device to be configured in a variety of different ways.

12. In reference to Claim 2, Ewering and Plog teach the limitations as applied to Claim 1 above. Ewering further teaches that each bus connection unit includes output circuitry connected to the bus portions to which the unit is connected, the output circuitry being optimized for the length of the bus portions concerned (See Pages 304-305 Section 2 'Target Architecture').

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Ewering using the multiplexers of Plog, resulting in the invention of Claim 2, because multiplexers are a type of switch and to allow multiple units to be on the same segment of bus by allowing them to be connected in parallel fashion by connecting one unit to the bus at a time (See Column 5 Lines 50-54 of Plog), and thus increase the functionality by allowing a single device to be configured in a variety of different ways.

13. In reference to Claim 3, Ewering and Plog teach the limitations as applied to Claim 1 above. Ewering further teaches that the bus portions are all equal in length (See Figure 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Ewering using the multiplexers of Plog, resulting in the invention of Claim 3, because multiplexers are a type of switch and to allow multiple units to be on the same segment of bus by allowing them to be connected in parallel fashion by connecting one unit to the bus at a time (See Column 5 Lines 50-54 of Plog), and thus increase the functionality by allowing a single device to be configured in a variety of different ways.

14. In reference to Claim 5, Ewering and Plog teach the limitations as applied to Claim 1 above. Ewering further teaches that a central arbitration unit arbitrates between the modules in order to grant access to the bus architecture (See Page 305 Column 1 Sections 3 and 4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Ewering using the multiplexers of Plog, resulting in the invention of Claim 5, because multiplexers are a type of switch and to allow multiple units to be on the same segment of bus by allowing them to be connected in parallel fashion by connecting one unit to the bus at a time (See Column 5 Lines 50-54 of Plog), and thus increase the functionality by allowing a single device to be configured in a variety of different ways.

15. In reference to Claim 12, Ewering and Plog teach the limitations as applied to Claim 1 above. Ewering further a computer system comprising the apparatus (See Figure 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Ewering using the multiplexers of Plog, resulting in the invention of Claim 12, because multiplexers are a type of switch and to allow multiple units to be on the same segment of bus by allowing them to be connected in parallel fashion by connecting one unit to the bus at a time (See Column 5 Lines 50-54 of Plog), and thus increase the functionality by allowing a single device to be configured in a variety of different ways.

16. Claims 4, 6, 7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ewering and Plog as applied to Claims 1 and 5 above, and further in view of US Patent Number 5,627,976 to McFarland et al. ("McFarland").

17. In reference to Claim 4, Ewering and Plog teach the limitations as applied to Claim 1 above. Ewering and Plog do not teach a primary pipelined bus and a secondary pipelined bus, the primary and secondary buses being interconnected by an interface. McFarland teaches a primary bus (See Figure 1 Number 20) and secondary bus (See Figure 1 Number 25) interconnected by an interface (See Figure 1 Number 45), a plurality of modules connected to the primary bus (See Figure 1 Numbers 32, 35,

and 37), and a plurality of modules connected to the secondary bus (See Figure 1 Numbers 40 and 42).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the dual bus system of McFarland with the partitioned bus structure of Ewering and Plog, resulting in the invention of Claim 4, because a dual bus system allows a very fast bus to interface with a much slower bus in a way that the high bandwidth of the former is maintained except when a device on the former and a device on the latter need to communicate (See Column 2 Lines 61-65 of McFarland) and because partitioned buses have proven to yield space efficient interconnection structures (See Page 304 Column 2 Section 2 'Target Architecture').

18. In reference to Claim 6, Ewering and Plog teach the limitations as applied to Claim 5 above. Ewering and Plog do not teach a primary pipelined bus and a secondary pipelined bus, the primary and secondary buses being interconnected by an interface. McFarland teaches a primary bus (See Figure 1 Number 20) and secondary bus (See Figure 1 Number 25) interconnected by an interface (See Figure 1 Number 45), a plurality of modules connected to the primary bus (See Figure 1 Numbers 32, 35, and 37), and a plurality of modules connected to the secondary bus (See Figure 1 Numbers 40 and 42).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the dual bus system of McFarland with the partitioned bus structure of Ewering and Plog, resulting in the invention of Claim 6, because a dual

bus system allows a very fast bus to interface with a much slower bus in a way that the high bandwidth of the former is maintained except when a device on the former and a device on the latter need to communicate (See Column 2 Lines 61-65 of McFarland) and because partitioned buses have proven to yield space efficient interconnection structures (See Page 304 Column 2 Section 2 'Target Architecture').

19. In reference to Claim 7, Ewering, Plog, and McFarland teach the limitations as applied to Claim 4 above. McFarland further teaches that the first plurality of modules are latency tolerant and the second plurality of modules are latency intolerant (See Figure 1, Column 2 Line 61 – Column 3 Line 12 and Column 5 Lines 21-32).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the dual bus system of McFarland with the partitioned bus structure of Ewering and Plog, resulting in the invention of Claim 7, because a dual bus system allows a very fast bus to interface with a much slower bus in a way that the high bandwidth of the former is maintained except when a device on the former and a device on the latter need to communicate (See Column 2 Lines 61-65 of McFarland) and because partitioned buses have proven to yield space efficient interconnection structures (See Page 304 Column 2 Section 2 'Target Architecture').

20. In reference to Claim 8, Ewering, Plog, and McFarland teach the limitations as applied to Claim 4 above. McFarland further teaches that the primary bus is one pipeline stage in length (See Figure 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the dual bus system of McFarland with the partitioned bus structure of Ewering and Plog, resulting in the invention of Claim 8, because a dual bus system allows a very fast bus to interface with a much slower bus in a way that the high bandwidth of the former is maintained except when a device on the former and a device on the latter need to communicate (See Column 2 Lines 61-65 of McFarland) and because partitioned buses have proven to yield space efficient interconnection structures (See Page 304 Column 2 Section 2 'Target Architecture').

21. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ewering and Plog as applied to Claim 1 above, and further in view of US Patent Number 5,128,926 to Perlman et al. ("Perlman").

22. In reference to Claim 9, Ewering and Plog teach the limitations as applied to Claim 1 above. Ewering and Plog do not teach that transactions involving data in excess of a predetermined size are split into a plurality of data packets of fixed size, said packets being independently arbitrated. Perlman teaches splitting a large packet into pieces which are smaller than the maximum packet size and transmitting the smaller packets separately (See Column 2 Lines 55-58).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Ewering and Plog with the packet splitting of Perlman, resulting in the invention of Claim 4, in order to relieve the computation

burden by reducing the probability of errors in transmission (See Column 2 Line 64 – Column 3 Line 14 of Perlman).

23. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ewering and Plog as applied to Claim 1 above, and further in view of US Patent Number 5,925,118 to Revilla et al. ("Revilla").

24. In reference to Claim 10 Ewering and Plog teach the limitations as applied to Claim 1 above. Ewering and Plog do not teach separate read, write, and transaction buses. Revilla teaches the use of separate read (See Figure 1 Number 34), write (See Figure 1 Number 32), and transaction buses (See Figure 1 Number 36).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Ewering and Plog with the split bus system of Revilla, resulting in the invention of Claim 10, in order to reduce the number of buses and, therefore, the number of connections required while still providing acceptable data throughput (See Column 1 Lines 19-23 and Column 2 Lines 17-31 of Revilla).

25. In reference to Claim 11 Ewering and Plog teach the limitations as applied to Claim 1 above. Ewering and Plog do not teach that the bus architecture has a width sufficient to permit read and write request transactions to alternate in successive system clock cycles. Revilla teaches the use of separate read (See Figure 1 Number 34), write

(See Figure 1 Number 32), and transaction buses (See Figure 1 Number 36) which have a width sufficient to permit read and write request transactions to alternate in successive system clock cycles (See Column 3 Lines 12-26).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Ewering and Plog with the split bus system of Revilla, resulting in the invention of Claim 11, in order to reduce the number of buses and, therefore, the number of connections required while still providing acceptable data throughput (See Column 1 Lines 19-23 and Column 2 Lines 17-31 of Revilla).

Drawings

26. The drawings are objected to as failing to comply with 37 CFR 1 .84(p)(5) because they include the following reference sign(s) not mentioned in the description: Figure 1 Numbers 1 and 2; Figure 13 Letters D and H; Figure 14 Numbers 28 and 29; Figures 15, 16, 17, 18, and 19 Number 30; Figure 21 Numbers 35, 36, and 37; Figure 22 Numbers 39, 40, 41, and 42; Figure 26 Numbers 56, and 57; Figure 28 Number 73; Figure 29 Number 84. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

27. The drawings are objected to as failing to comply with 37 CFR 1 .84(p)(4) because reference character "A" has been used to designate both "start" in Figure 13 and "assign initial stack positions" on Page 17 Lines 25-26. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

28. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "B" has been used to designate both "assign initial stack positions" in Figure 13 and "receive respective transaction requests" on Page 17 Line 32 – Page 18 Line 2. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

29. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "C" has been used to designate both "receive transaction request" in Figure 13 and "determine highest priority level" on Page 18 Lines 5-8. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Conclusion

30. The following prior art made of record and not relied upon is considered pertinent to Applicant's disclosure: US Patent Number 5,778,250 to Dye; US Patent Number 5,948,098 to Leung et al.; US Patent Number 6,247,161 to Lambrecht et al.; US Patent Number 6,263,389 to LaBerge; "Hardware Synthesis for Stack type Partitioned-Bus Architecture" by Kim et al.; and "Constrained Register Allocation in Bus Architectures" by Frank et al.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The Examiner can normally be reached on Monday-Thursday (7-3:30), Alt. Fridays (7-2:30).

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul R. Myers

PAUL R. MYERS
PRIMARY EXAMINER

TJC

Thomas J. Cleary
Patent Examiner
Art Unit 2111